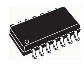
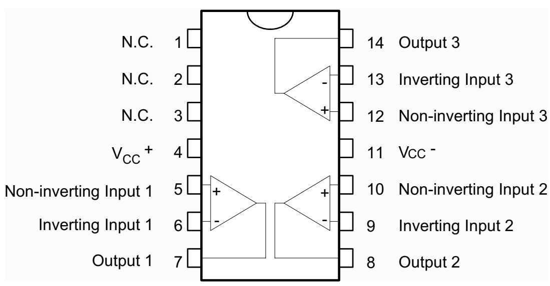
High-speed Low Power Triple Operational Amplifier

- Low supply current: 4.5mA
- High-speed: 150MHz - 110V/µs
- Unity gain stability
- Low offset voltage: 4mV
- Low noise: 4.2nV/√Hz
- Low cost
- Specified for 600Ω and 150Ω loads
- High video performances:
  Differential gain: 0.03%
  Differential phase: 0.07°
  Gain flatness: 6MHz, 0.1dB max. 0 10dB gain
- High audio perform
- ESD tolerance: 2kV



D
SO-14
(Plastic Micropackage)

Pin Connections (top view)



Description

The TSH93 is a triple low power high frequency op-amp, designated for high quality video signal processing. The device offers an excellent speed consumption ratio with 4.5mA per amplifier for 150MHz bandwidth.

High slew rate and low noise make it also suitable for high quality audio applications.

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TSH93ID/IDT	-40°C, +125°C	SO-14	Tube or Tape & Reel	H93
TSH93IYD/IYD		SO-14 (automotive grade level)	Tube or Tape & Reel	H93Y

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (1)	14	V
V_{id}	Differential Input Voltage (2)	±5	V
V_i	Input Voltage (3)	-0.3 to 12	V
T_{oper}	Operating Free-Air Temperature range	-40 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C

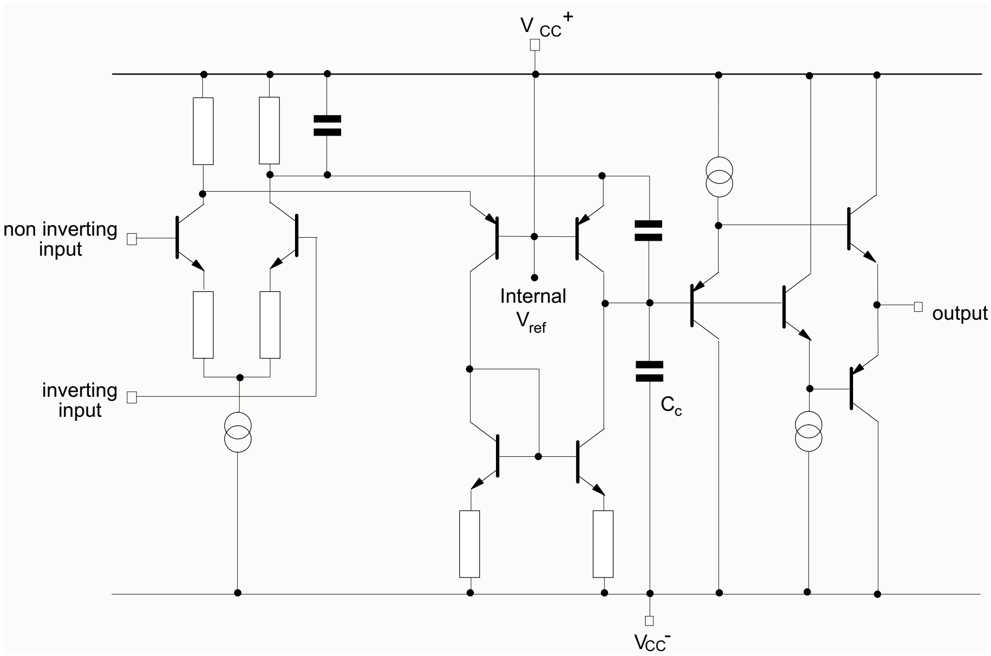
1. All voltages values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltages must never exceed V_{CC}^+ +0.3V.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	7 to 12	V
V_{ic}	Common Mode Input Voltage Range	V_{CC}^- +2 to V_{CC}^+ -1	V

2 Schematic Diagram

Figure 1. Schematic diagram (1/3)



3 Electrical Characteristics

Table 3. V_{CC}^{+} = 5V, V_{CC}^{-} = -5V, T_{amb} = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage $T_{min.} \leq T_{amb} \leq T_{max.}$			4 6	mV
I_{io}	Input Offset Current $T_{min.} \leq T_{amb} \leq T_{max.}$		1	2 5	µA
I_{ib}	Input Bias Current $T_{min.} \leq T_{amb} \leq T_{max.}$		5	15 20	µA
I_{CC}	Supply Current (per amplifier, no load) $T_{min.} \leq T_{amb} \leq T_{max.}$		4.5	6 8	mA
CMR	Common-mode Rejection Ratio V_{ic} = -3V to +4V, V_o = 0V $T_{min.} \leq T_{amb} \leq T_{max.}$	80 70	100		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = ±5V to ±3V $T_{min.} \leq T_{amb} \leq T_{max}$	60 50	75		dB
Avd	Large Signal Voltage Gain R_L = 100Ω, Vo = ±2.5V $T_{min.} \leq T_{amb} \leq T_{max.}$	57 54	70		dB
V_{OH}	High Level Output Voltage V_{id} = 1V R_L = 600Ω R_L = 150Ω $T_{min.} \leq T_{amb} \leq T_{max.}$ - R_L = 150Ω	3 2.5 2.4	3.5 3		V
V_{OL}	Low Level Output Voltage V_{id} = 11V R_L = 600Ω R_L = 150Ω $T_{min.} \leq T_{amb} \leq T_{max.}$ - R_L = 150Ω		-3.5 -2.8	-3 -2.5 -2.4	V
I_o	Output Short Circuit Current - Vid = ±1V Source Sink $T_{min.} \leq T_{amb} \leq T_{max.}$ - Source Sink	20 20 15 15	36 40		mA
GBP	Gain Bandwidth Product A_{VCL} = 100, R_L = 600Ω, C_L = 15pF, f = 7.5MHz	90	150		MHz
f_T	Transition Frequency		90		MHz
SR	Slew Rate V_{in} = -2 to +2V, A_{VCL} = +1, R_L = 600Ω, C_L = 15pF	62	110		V/µs
e_n	Equivalent Input Voltage Noise R_s = 50Ω, f = 1kHz		4.2		nV/√Hz
φm	Phase Margin A_{VM} = +1		35		Degrees
V_{O1}/V_{O2}	Channel Separation f = 1MHz to 10MHz		65		dB

Table 3. $V_{CC}^{+} = 5V$, $V_{CC}^{-} = -5V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Gf	Gain Flatness f = DC to 6MHz, $A_{VCL} = 10dB$			0.1	dB
THD	Total Harmonic Distortion f = 1kHz, $V_o = \pm 2.5V$, $R_L = 600\Omega$		0.01		%
ΔG	Differential Gain f = 3.58MHz, $A_{VCL} = +2$, $R_L = 150\Omega$		0.03		%
$\Delta\varphi$	Differential Phase f = 3.58MHz, $A_{VCL} = +2$, $R_L = 150\Omega$		0.07		Degrees

Table 4. $V_{cc}^{+} = \pm 15V$, $T_{amb} = 25°C$ (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	$R_L = 600\Omega$	3.2	V/mV
I_{CC}	No load / Ampli	5.2	mA
V_{icm}		-3 to 4	V
V_{OH}	$R_L = 600\Omega$	+3.6	V
V_{OL}	$R_L = 600\Omega$	-3.6	V
I_{sink}	$V_o = 0V$	40	mA
I_{source}	$V_o = 0V$	40	mA
GBP	$R_L = 600\Omega$, $C_L = 15pF$	147	MHz
SR	$R_L = 600\Omega$, $C_L = 15pF$	110	V/µs
ϕm	$R_L = 600\Omega$, $C_L = 15pF$	42	Degrees

4 Printed Circuit Layout

As for any high frequency device, a few rules must be observed when designing the PCB to get the best performances from this high speed op-amp.

From the most to the least important points:

- Each power supply lead has to be bypassed to ground with a 10nF ceramic capacitor very close to the device and a 10µF capacitor.
- To provide low inductance and low resistance common return, use a ground plane or common point return for power and signal.
- All leads must be wide and as short as possible especially for op-amp inputs. This is in order to decrease parasitic capacitance and inductance.
- Use small resistor values to decrease time constant with parasitic capacitance.
- Choose component sizes as small as possible (SMD).

On output, decrease capacitor load so as to avoid circuit stability being degraded which may cause oscillation. You can also add a serial resistor in order to minimize its influence.

Figure 2. Input offset voltage drift vs. temperature

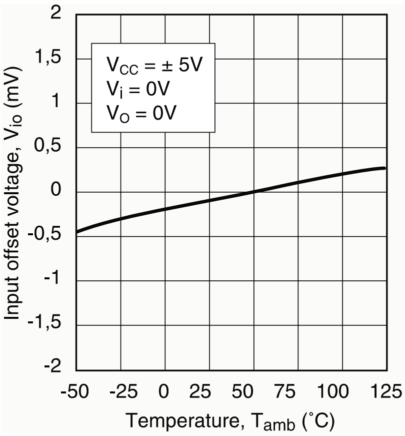


Figure 3. Static open loop voltage gain

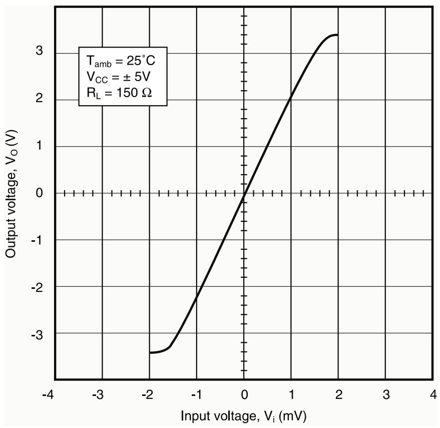


Figure 4. Large signal follower response

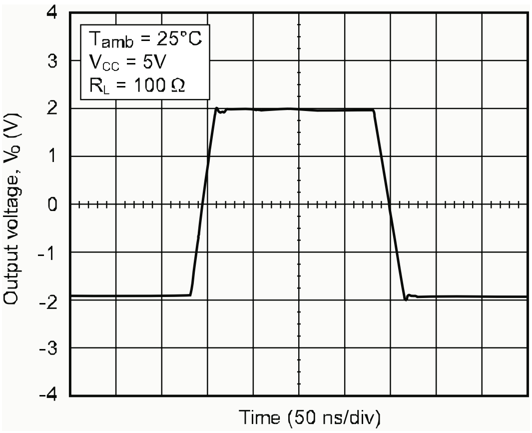


Figure 5. Small signal follower response

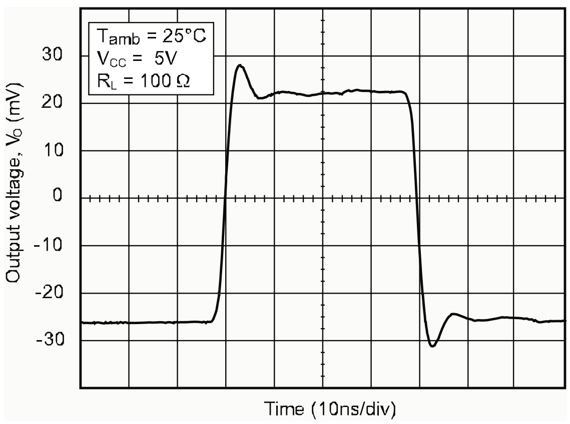


Figure 6. Open loop frequency response & phase shift

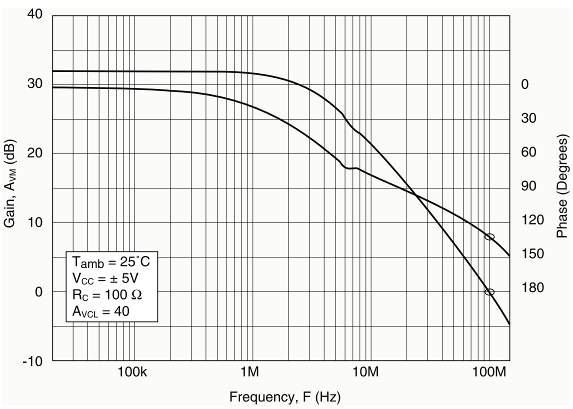


Figure 7. Close loop frequency response

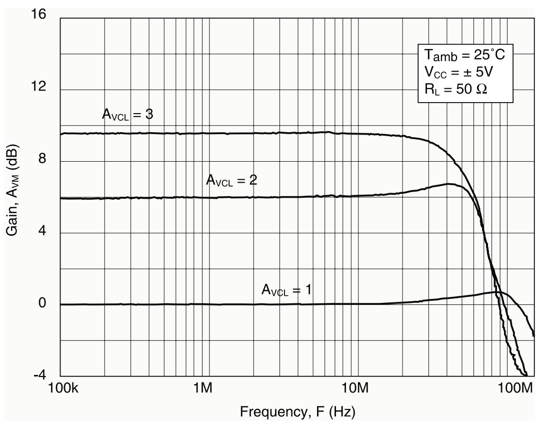


Figure 8. Audio bandwidth frequency - Response & phase shift (TSH93 vs. standard 15MHz audio op-amp)

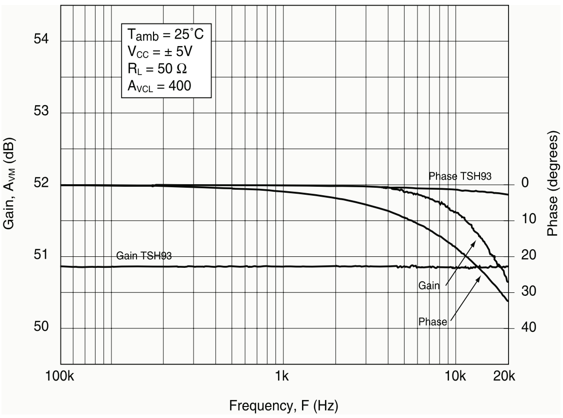


Figure 9. Gain flatness & phase shift vs. frequency

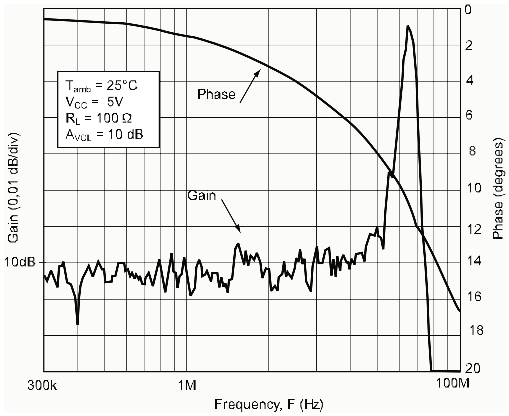


Figure 10. Cross talk isolation vs. frequency (SO-14 package)

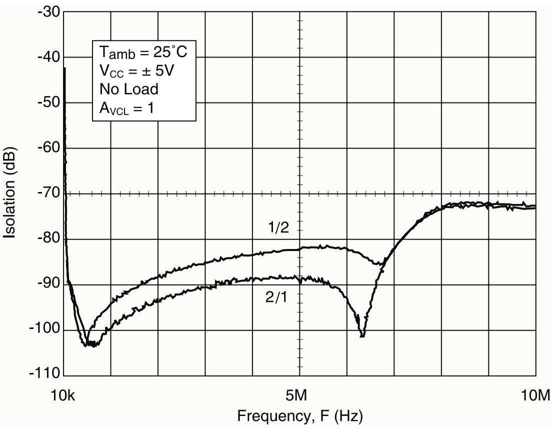


Figure 11. Cross talk isolation vs. frequency (SO-14 package)

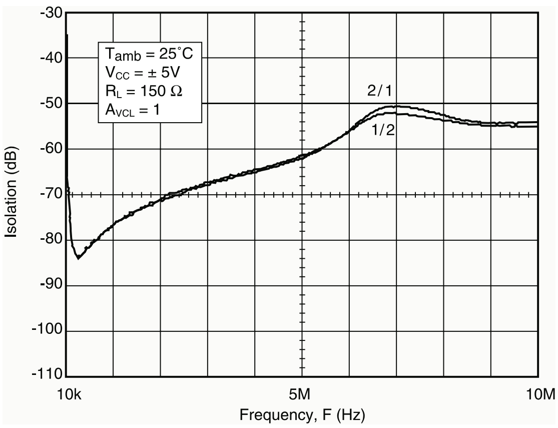


Figure 12. Differential input impedance vs. frequency

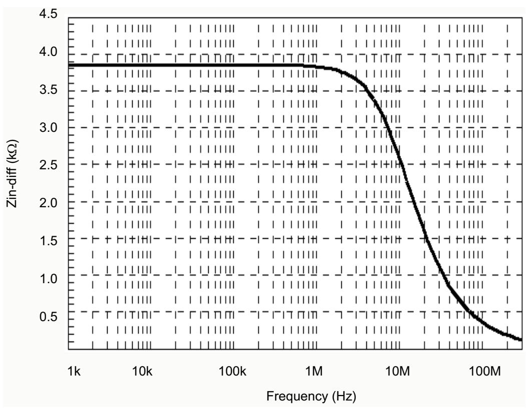
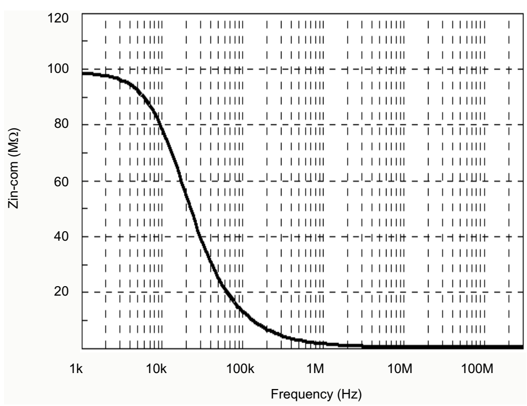


Figure 13. Common input impedance vs. frequency



5 Macromodels

Note: Note: Please consider following remarks before using this macromodel:

All models are a trade-off between accuracy and complexity (i.e. simulation time).

Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.

A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.

Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc.) or even worse: outside of the device operating conditions (Vcc, Vicm, etc.) are not reliable in any way.

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Applies to: TSH93I
** Standard Linear Ics Macromodels, 1997.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVEPOWER SUPPLY
* 5 NEGATIVE POWER SUPPLY
.SUBCKT TSH93 1 3 2 4 5(analog)
*******************************************************
.MODEL MDTH D IS=1E-8 KF=1.809064E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E-01
RIN 15 16 2.600000E-01
RIS 11 15 3.645298E-01
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0.000000E+00
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-03
CPS 11 15 2.986990E-10
DINN 17 13 MDTH 400E-12
VIN 17 5 2.000000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 1.000000E+00
FCP 4 5 VOFP 3.500000E+00
FCN 5 4 VOFN 3.500000E+00
FIBP 2 5 VOFP 1.000000E-02
FIBN 5 1 VOFN 1.000000E-02
* AMPLIFYING STAGE
FIP 5 19 VOFP 2.530000E+02
```

```
FIN 5 19 VOFN 2.530000E+02
RG1 19 5 3.160721E+03
RG2 19 4 3.160721E+03
CC 19 5 2.00000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 1.504000E+03
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 1.400000E+03
VINM 5 27 5.000000E+01
***********************
RZP1 5 80 1E+06
RZP2 4 80 1E+06
GZP 5 82 19 80 2.5E-05
RZP2H 83 4 10000
RZP1H 83 82 80000
RZP2B 84 5 10000
RZP1B 82 84 80000
LZPH 4 83 3.535e-02
LZPB 84 5 3.535e-02
EOUT 26 23 82 5 1
VOUT 23 5 0
ROUT 26 3 35
COUT 3 5 30.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.361965E+00
DON 24 19 MDTH 400E-12
VON 24 5 2.361965E+00
.ENDS
```

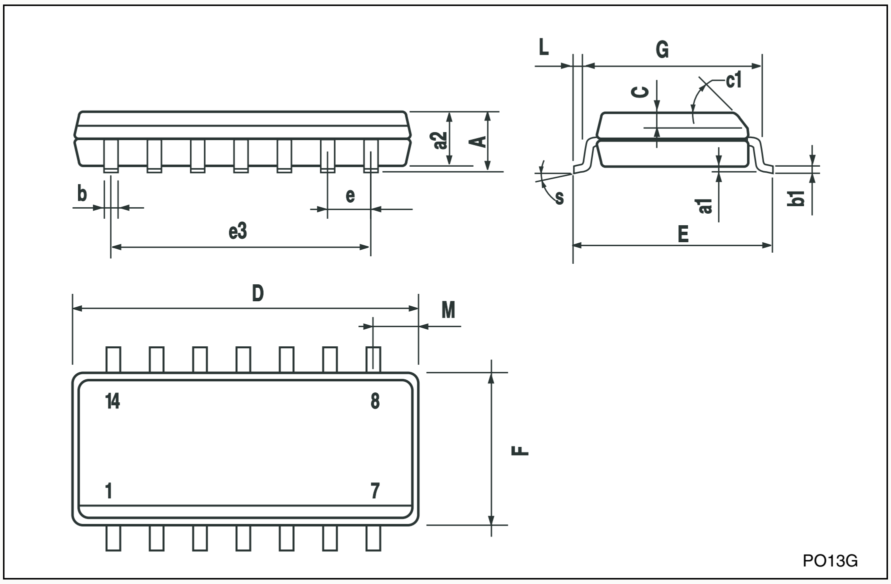
6 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

6.1 SO-14 Package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					



7 Revision History

Date	Revision	Changes
Oct. 2000	1	First Release
Aug. 2005	3	1 - PPAP references inserted in the datasheet see *Table : Order Codes on page 1*.